Transposing Conductors in Signal Buses to Reduce Nearest-Neighbor Crosstalk

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Abstract—**A conductor layout technique is described that reduces nearest-neighbor crosstalk for multiconductor signal buses with applications in high-speed digital and microwave pulse integrated circuits. Periodic transposition of conductors in a bus increases the average spacing of formerly nearest neighbors and thus decreases their capacitive and inductive coupling compared with ordinary parallel conductors. A conductor transposition pattern is evaluated for crosstalk, propagation delay, and chip area. SPICE simulations demonstrate that conductor transposition reduces, in certain situations, near- and far-end nearest-neighbor crosstalk by roughly 40% compared with parallel conductors. Quantitative guidelines are developed for reducing nearest-neighbor crosstalk in a transposed five-conductor bus, including effects of signal rise time, source resistance, load capacitance, and bus length.**

I. Introduction

In high-speed digital and broadband microwave pulse integrated circuits (IC's), crosstalk is the undesirable electromagnetic field coupling of a signal on one conductor to a neighboring conductor in a multiconductor signal bus. If the crosstalk signal is too large, then logic circuits on neighboring conductors are triggered falsely. To prevent logic errors from occurring, it is necessary to employ crosstalk-reduction techniques in designing circuitry.

At signal frequencies where the quasi-TEM approximation is valid, near-end crosstalk is minimized by reducing inductive and/or capacitive coupling between conductors, and far-end crosstalk is minimized by reducing the difference of inductive and capacitive coupling [1]. Several techniques are available in integrated circuit design to reduce crosstalk, such as increasing the spacing between conductors in a bus and placing grounded conductors between the signal conductors [2], [3]. Another crosstalk-reduction technique covers the conductors with a thin, high-dielectric-constant material topped with a metal ground plane to provide a relatively smaller ratio of mutual capacitance between conductors to ground capacitance [2]. This technique consumes two layers of metallization along the entire bus length, providing only half the wiring density were the second metallization layer also used for signal interconnections. Special fabrication procedures are used in the substrate compensation technique for reducing crosstalk [4]. A two-layer substrate, consisting of an upper layer with a much higher dielectric constant than the lower layer, provides equal even and odd mode propagation velocities and thus reduces crosstalk. Another crosstalk reduction method requiring special fabrication techniques is based on using a wide notch in the dielectric substrate between conductors [5]. The notch reduces the mutual capacitance significantly between the conductors.

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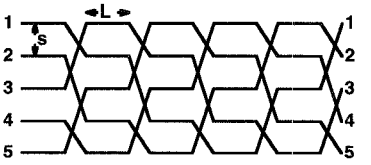

Fig. 1. Example of conductor transposition for five lines.

In an alternative crosstalk-reduction technique requiring only a standard two-level metal process for fabrication, it is proposed that the conductors be segmented periodically along their length and that they be transposed at the interface between segments (Fig. 1). Thus, no two signal paths are highly-coupled nearest neighbors for the entire bus length. Historically, conductor transposition was used by telephone utilities for balanced, open lines strung between telephone poles [6], [7]. These thousand-kilometer-long lines are periodically transposed so that no two pairs of conductors are nearest neighbors for a significant fraction of a wavelength at audio frequencies.

In high-speed digital and high-frequency microwave pulse IC's, it is possible to use conductor transposition to increase the average spacing between two formerly nearest-neighbor signal paths, thus reducing the average mutual capacitance and inductance between them. For example, in a transposed-conductor data bus on a digital chip, weaving one signal path between all the others spreads and dilutes its crosstalk energy among all the conductors. Conversely, in a parallel-conductor bus, the crosstalk energy is concentrated at the nearest neighbors of the driven line with a higher intensity than if spread among all conductors. Transposition becomes less effective at crosstalk reduction as the number of simultaneously-switching lines increases. In the limit of all but one line switching simultaneously, the amount of crosstalk for the transposed lines is about the same as for ordinary parallel lines. However, for some circuitry, only a few lines at a time switch simultaneously. A simple case is the use of a binary Gray [8] code to send information along the lines, in which just one line of many undergoes a signal transition at any given time. Thus, as will be shown, the conductor transposition technique is effective at reducing crosstalk in certain circumstances.

Crosstalk reduction through increased conductor spacing is discussed as relevant to transposed conductor buses. Design

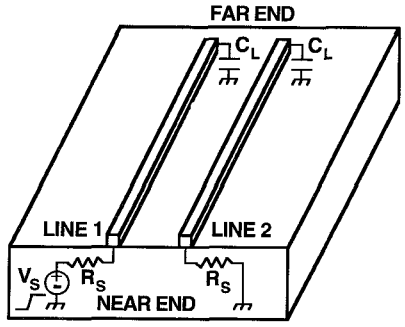

Fig. 2. Two lines of a multiconductor signal bus.

goals for conductor transposition are stated and a suitable transposition pattern is developed. Concerns are addressed in modeling transposed lines at high frequencies. The SPICE3 [9] simulation program is used to analyze the effectiveness of transposed lines at reducing near- and far-end nearest-neighbor crosstalk for several different terminations and lengths. Ordinary and transposed buses are compared for signal delay and distortion. Quantitative design guidelines are developed for transposed buses to achieve significant nearest-neighbor crosstalk reduction.

II. Reducing Crosstalk by Increasing Conductor Spacing

Transposed conductor buses depend on the increased average spacing between two conductors to reduce the crosstalk intensity. Fig. 2 shows two lines of a multiconductor bus in an IC. The output voltage and resistance of a logic gate driving line 1 at the near end are represented by V_S and R_S, respectively. Capacitor C_L represents the input capacitance of a GaAs MESFET or high-speed MOSFET gate at the far end of the line. As the voltage step generated by V_S propagates toward the load along line 1, backward traveling crosstalk, proportional to $C_m Z_o + L_m/Z_o$, is introduced into line 2, where C_m and L_m are the mutual capacitance and inductance, respectively, between the lines and Z_o is the characteristic impedance [1]. Increasing the line separation will reduce C_m and L_m and thus reduce the backward crosstalk at the near end on line 2 [10].

Also generated in line 2 is the forward traveling crosstalk, which is proportional to $C_m Z_o - L_m/Z_o$ [1], [11] and appears at the far end of the line. This difference is negative for an inhomogeneous dielectric as studied here in an IC. Simultaneously, the pulse on line 1 reaches the far end, and, for the pulse rise times and load capacitances studied here, observes a nearly unity voltage reflection coefficient. Thus, a pulse traveling toward the source is created at the far end of line 1 with nearly the amplitude of the original, incoming pulse. Consequently, a large reverse crosstalk traveling toward the load and proportional to $C_m Z_o + L_m/Z_o$ is also introduced at the far end of line 2. This crosstalk dominates the negative crosstalk at the end of line 2 and their sum is thus a positive value. As the conductor separation is made larger, the far end crosstalk will also decrease.

III. Conductor Transposition Patterns

For maximum effectiveness in reducing crosstalk, the conductors should be transposed so that any two signal paths have a large average spacing. The transpositions should not introduce a significant amount of additional mutual capacitance or mutual inductance between conductors where one crosses another. To maintain a compact circuit layout, the transpositions should utilize as little additional chip area as possible compared with the conventional parallel bus. Finally, to reduce the effort required to design the layout, the same crossover pattern should be used at each transposition.

To meet these design goals, a transposition algorithm is developed for an n-conductor bus. The ith element of the transposition vector T describes which conductor to the left of the transposition is connected to the ith conductor on the right. For n even

$$T_i = \begin{cases} 1, & i = 2 \\ i-2, & i > 2,\ i \text{ even} \\ i+2, & i < n-1,\ i \text{ odd} \\ n, & i = n-1 \end{cases}$$

and for n odd

$$T_i = \begin{cases} 1, & i = 2 \\ i-2, & i > 2,\ i \text{ even} \\ i+2, & i < n,\ i \text{ odd} \\ n-1, & i = n. \end{cases}$$

Fig. 1 shows this transposition pattern for $n = 5$. Table I summarizes properties of this transposition algorithm for $n = 3$–6. Periodically, after passing through several transpositions, the conductors will be in the same physical order as they are at the left end of the bus. The distance between segments with conductors in the same order, specified in terms of the segment length L, is called the physical repeat distance. After passing through several transpositions, the conductors will be in the reverse physical order that they have at the left end of the bus. The distance separating these segments is called the electrical repeat distance, since the electrical behavior for a segment with reverse-ordered conductors is the same as for normally-ordered conductors. Also listed are the spacing for each segment between the pair of conductors having the smallest average spacing (worst case) and the worst-case average spacing itself. These spacings are specified in terms of s, the spacing between nearest-neighbor conductors. In the limit of large n, the worst-case average spacing approaches $2s$. Fig. 3 details the use of a two-level metallization pattern to form the crossovers necessary for five-line conductor transposition. The crossover pattern is easily extended to other numbers of conductors. Small squares indicate vias in the dielectric between metal levels.

IV. Modeling of Interconnect

A five-conductor bus with dimensions typical for a high-speed GaAs IC is considered. This bus, modeled on a 0.5-mm-thick GaAs substrate, has aluminum lines 3-μm-wide, 0.3-μm-thick, with 3-μm edge-to-edge separation. The clock frequency of high-speed IC's ranges up to a few gigahertz with rise times as short as 100 ps [12], providing a frequency

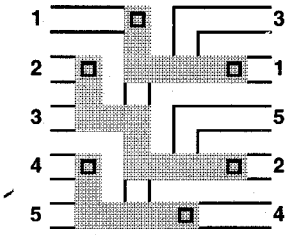

Fig. 3. Example of transposition crossovers for five conductors. The shaded regions represent the second-level metal.

TABLE I
CHARACTERISTICS OF TRANSPOSED LINES

n	T	physical repeat distance	electrical repeat distance	worst-case spacing	worst-case average spacing
3	3 1 2	$3L$	$3L$	s,s,$2s$	$1.33s$
4	3 1 4 2	$4L$	$2L$	s,$2s$,s,$2s$	$1.5s$
5	3 1 5 2 4	$5L$	$5L$	s,$2s$,s,$2s$,$2s$	$1.6s$
6	3 1 5 2 6 4	$6L$	$3L$	s,$2s$,$2s$,s,$2s$,$2s$	$1.67s$

spectrum extending to about 10 GHz. For this bus, the quasi-TEM modeling approach is sufficient [13]. The capacitance matrix is evaluated using the moment-method based LINPAR software [14], [15].

Results of modeling the five-conductor bus, based on the method in [16], are that the self- and mutual-inductances change by less than one percent at 10 GHz from their low-frequency values. Thus, their low-frequency values are used. The line resistance increases by less than two percent over this frequency range, and thus the d.c. value is used. Although the mutual resistance values increase significantly over the frequency range, they are still very small compared with the impedance of the mutual inductances at 10 GHz and the self-resistance of each line, and thus are neglected.

The coupled lines are modeled as cascaded lumped-π LCR networks [17], since the SPICE3 circuit simulation program does not have a built-in model for coupled lines. Results of a SPICE3 simulation of a single 10-mm-long conductor of the five-conductor bus using five sections of the lumped-π model agree well with a SPICE3 simulation using the built-in LTRA single-conductor lossy-line model. The step pulse rise time (0–100%) is 100 ps, the source resistance is 125 Ω, and the load capacitance is 64 fF. The excellent agreement suggests that using five sections of lumped-π networks to model coupled lines is sufficient to avoid ringing [17] for lines up to 10 mm in length with pulses having rise times of at least 100 ps.

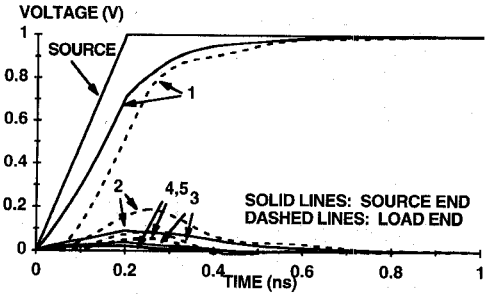

Fig. 4. Voltages at ends of the parallel five-conductor bus with line 1 driven.

To evaluate the amount of crosstalk in the 5-mm-long parallel bus, SPICE3 is used to simulate the bus as five cascaded lumped-π networks. At the near end of each line there is a 125-Ω resistance to ground to represent the output impedance of GaAs DCFL logic gates. A 1-V 200-ps rise time step pulse is placed in series with the 125-Ω resistance for line 1. The far ends of the lines are terminated with 64 fF capacitances to represent the input impedance of logic gates being driven. Fig. 4 shows the voltages at the source and load ends of the bus. Crosstalk on line 2, with respect to the 1-V signal source, is 9% at the source end and 19% at the load end. Crosstalk on line 3 is 4% at the source end and 9% at the load end. This significant reduction in crosstalk, obtained by increasing the separation between driven and coupled lines by just one line, is the basis for the transposed-line crosstalk reduction technique.

V. EFFECTIVENESS OF TRANSPOSITION IN REDUCING CROSSTALK

To analyze the performance of transposed buses, five transpositions are added to the parallel bus of Section IV. Five transpositions are the fewest that can be used on a five-conductor bus while providing the output lines in the same physical order as the input lines. Using integer multiples of five transpositions will contribute additional parasitic inductance and capacitance without providing an increase in average spacing between conductors. The transpositions are included as lumped-LCR networks in the SPICE3 simulations. Simulation results provide design guidelines for achieving crosstalk reduction.

The five-conductor transposition shown in Fig. 3 is used with a 0.5-μm polyimide dielectric between the first- and second-level metal. The second-level metal has the same cross-sectional dimensions as the first-level metal discussed earlier. The additional space needed for the transposed-line bus is that for the crossovers, which consume only a 21-μm length of second-level metal. This is an efficient use of chip area, considering that the crossovers are widely spaced along the bus length. The capacitance matrix describing the transposition is determined using a three-dimensional graded-mesh version of the finite-difference solution technique for Laplace's equation in [18].

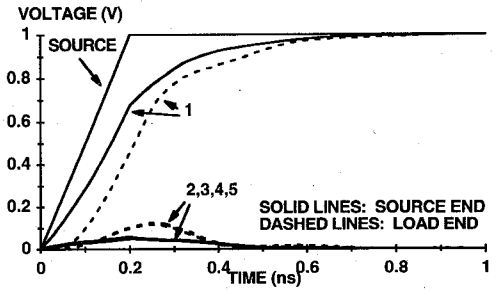

Fig. 5. Voltages at ends of the transposed five-conductor bus with line 1 driven.

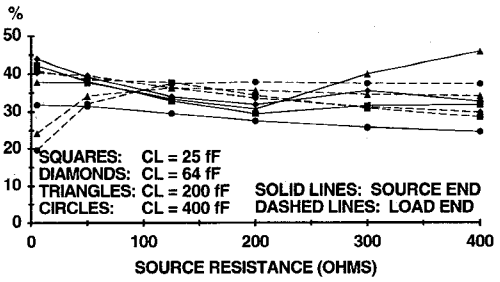

Fig. 6. Percentage reduction in nearest-neighbor crosstalk achieved by transposing conductors in the five-conductor bus for several values of R_S and C_L. Line 1 is driven.

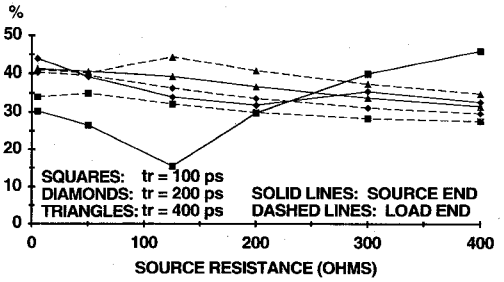

Fig. 7. Percentage reduction in nearest-neighbor crosstalk achieved by transposing conductors in the five-conductor bus for several values of R_S and pulse rise time t_r. Line 1 is driven.

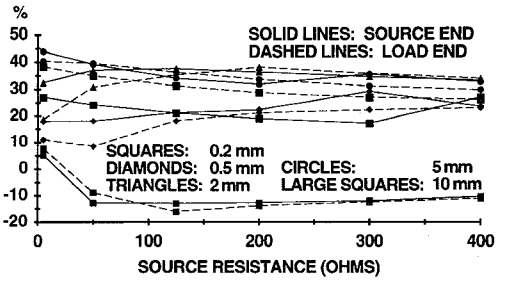

Fig. 8. Percentage reduction in nearest-neighbor crosstalk achieved by transposing conductors in the five-conductor bus for several values of R_S and bus length. Line 1 is driven.

The inductance of each straight segment composing the transposition is estimated from the inductance per unit length using a computer program based on the method in [16]. The mutual inductance between parallel segments and between overlapping conductor segments is also estimated using the same program. The inductance of the right-angle bends is estimated as the inductance of a conductor having the same length as the bend when straightened [19]. The solid aluminum plugs in the via holes, 0.5 μm thick with 1 $\times$ 1-μm^2 cross-sectional area, have negligible inductance using [20, p. 31] and have negligible resistance. The series resistance for each conductor in the transposition is also negligible.

To demonstrate the effectiveness of bus transposition in reducing nearest-neighbor crosstalk, five equally-spaced transpositions are inserted in the parallel bus previously simulated while maintaining an overall length of 5 mm. Fig. 5 shows the voltages at the source and load ends of the bus. The crosstalk at the source end is roughly the same at 6% for all lines, which is a 34% reduction in near-end nearest-neighbor crosstalk compared with the parallel-line bus. For the load end, the crosstalk is roughly the same at 12% for all lines, which is a 36% reduction in far-end nearest-neighbor crosstalk compared with the parallel-line bus.

Fig. 6 provides quantitative results useful in the design of transposed buses. Presented is the percentage reduction in nearest-neighbor crosstalk achieved by the 5-mm-long transposed bus in comparison with the parallel bus. Line 1 is driven with a 1-V, 200-ps rise time voltage step through the source resistance. The source resistance is varied from 5–400 Ω and the load capacitance is varied from 25–400 fF. Resistance and capacitance values much larger than these are not used since the rise time of the output signal on line 1 will exceed 1 ns, much greater than the signal source rise time.

More design guidelines are presented in Fig. 7, where the crosstalk reduction capability of the 5-mm-long transposed bus in relation to the parallel bus is plotted versus source resistance and signal source rise time. Line 1 is driven and the load capacitance is 64 fF.

Fig. 8 is a plot of the nearest-neighbor crosstalk reduction capability of the transposed bus over the parallel bus versus source resistance and bus length. Bus length is limited to 10 mm, corresponding to the edge-to-edge distance across a large IC. The signal source has a 200-ps-rise time and the load capacitance is 64 fF. The 0.2-mm-long transposed bus has more crosstalk than the parallel bus, since the additional capacitance and inductance in the transposition increase crosstalk more than the increased average conductor spacing reduces crosstalk. Thus, for very short buses, it is preferable to use ordinary parallel buses.

The amount of distortion and delay suffered by the signal while propagating along the bus is also of interest. Fig. 9 shows the voltages at both ends of the driven line (line 1) for five-conductor transposed and parallel buses of several lengths. The signal source rise time is a fast, 100-ps edge, the source resistance is 125 Ω, and the load capacitance is 64 fF. For the short, 0.105-mm buses, there is essentially no difference in the results. For the load end of the 10 mm buses, the transposed bus has about the same waveform shape as the parallel bus except for a roughly 10% smaller amplitude. One cause for the smaller amplitude is the additional capacitance and inductance contributed by the transpositions. The other cause is that in the parallel bus, the signal travels exclusively on line 1, which has a lower total capacitance and thus shorter delay than lines 2–4, whereas in the transposed bus, the signal propagates along the higher-capacitance lines 2–4 for part of the bus length. This

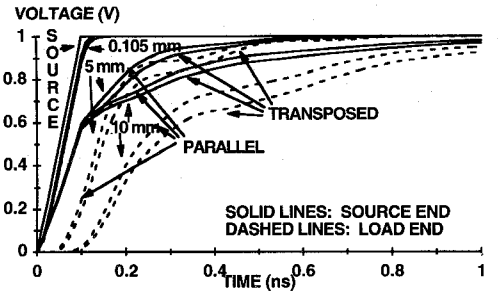

Fig. 9. Comparison of input and output voltages of the driven line for the parallel and transposed five-conductor buses of several lengths. Line 1 is driven.

second explanation is validated with the results of simulations of the same two 10-mm-long buses but with line 3 driven instead of 1. The output amplitude of the parallel bus is about 4% smaller than that of the transposed bus, even though the transposed bus has the additional capacitance and inductance of the transpositions. The output waveforms of the transposed buses with line 1 or line 3 driven are essentially the same, which indicates a potential advantage of the transposed bus over the ordinary parallel bus: There is better matching of the pulse waveforms at the output of a transposed bus for indentical input pulses. This feature may reduce signal timing skew in high-speed IC's.

For the five-conductor, 5-mm-long buses driven with a 200-ps rise time pulse and having 125-Ω source resistance and 64-fF load capacitance, the transposed bus provides less crosstalk reduction as the number of lines driven increases. SPICE3 simulations show that when both lines 2 and 4 are driven simultaneously, the crosstalk reduction is 31 and 34% for near- and far-end crosstalk on line 3, respectively. When lines 1, 2, 4, and 5 are driven simultaneously, near- and far-end crosstalk on line 3 are both reduced by only 6%.

VI. Conclusion

Periodic transposition of conductors in a five-line signal bus is shown to reduce near- and far-end nearest-neighbor crosstalk compared with an ordinary parallel-line bus. The crosstalk signal energy in the transposed case is spread and diluted among all conductors, rather than being concentrated at the two nearest-neighbors as with parallel lines. The transposed bus is analyzed for crosstalk reduction effectiveness over a parallel bus and design guidelines are developed in terms of pulse rise time, source resistance, load capacitance, and bus length. Crosstalk reduction is expected to be even greater if a transposition algorithm is used that increases the average spacing of formerly nearest-neighbors beyond that developed here. Although only a five-conductor bus is simulated using SPICE3, it is expected that the crosstalk-reduction effectiveness will improve as the number of conductors in the bus increases. Transposed-line buses possibly may have applications for high-speed GaAs direct-coupled FET logic circuits and other circuitry with small noise margins.

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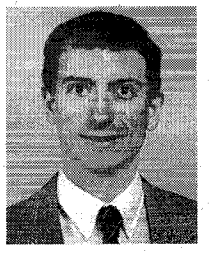

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